CLAIMS

What is claimed is:

Sub A3

1. An apparatus comprising:

a configuration storage containing configuration parameters to configure a processor in one of a normal execution mode and an isolated execution mode;

an access generator circuit coupled to the configuration storage to generate an isolated access signal using at least one of the configuration parameters and access information in a transaction, the isolated access signal being asserted when the processor is configured in the isolated execution mode; and

a bus cycle decoder coupled to the access generator circuit to generate an isolated bus cycle corresponding to a destination in the transaction using the asserted isolated access signal and the access information.

2. The apparatus of claim 1 wherein the configuration parameters include an isolated setting and an execution mode word.

3. The apparatus of claim 1 wherein the destination in the transaction is one of an isolated memory area in a memory external to the processor, an isolated register, and an isolated state.

4. The apparatus of claim 3 wherein the access information comprises a physical address and an access type.

5. The apparatus of claim 4 wherein the configuration storage comprises:

a register to contain the isolated setting for defining the isolated memory area.

6. The apparatus of claim 5 wherein the isolated setting is one of a mask value, a base value, and a length value.

7. The apparatus of claim 6 wherein the configuration storage further comprises:

a processor control register to contain the execution mode word, the execution mode word being asserted when the processor is configured in the isolated execution mode.

8. The apparatus of claim 7 wherein the access generator circuit comprises:

an address detector to detect if the physical address is within the isolated memory area defined by the isolated setting.

9. The apparatus of claim 8 wherein the isolated bus cycle is one of a data access cycle, a control access cycle, and a logical processor access cycle.

10. The apparatus of claim 9 wherein the data access cycle is generated when the access type is a memory reference to the isolated memory area.

11. The apparatus of claim 9 wherein the isolated register is in a chipset external to the processor.

12. The apparatus of claim 11 wherein the control access cycle is generated when the access type is an input/output reference to the isolated register.

13. The apparatus of claim 9 wherein the logical processor access cycle is generated when the access type is one of a logical processor entry to and a logical processor withdrawal from the isolated state.

14. The apparatus of claim 13 wherein the logical processor entry to the isolated state updates a logical processor counter in the chipset in a first direction.

15. The apparatus of claim 13 wherein the logical processor withdrawal from the isolated state updates a logical processor counter in the chipset in a second direction.

16. A method comprising:

configuring a processor in one of a normal execution mode and an isolated execution mode using a configuration storage in the processor, the configuration storage containing configuration parameters;

asserting an isolated access signal by an access generator circuit using at least one of the isolated area parameters and access information in a transaction when the processor is configured in the isolated execution mode; and

generating an isolated bus cycle corresponding to a destination in the transaction by a bus cycle decoder using the asserted isolated access signal and the access information.

17. The method of claim 16 wherein the configuration parameters include an isolated setting and an execution mode word.

18. The method of claim 16 wherein the destination in the transaction is one of an isolated memory area in a memory external to the processor, an isolated register, and an isolated state.

19. The method of claim 18 wherein the access information includes a physical address and an access type.

20. The method of claim 19 wherein configuring comprises:

defining the isolated memory area using the isolated setting contained in a register.

21. The method of claim 20 wherein the isolated setting is one of a mask value a base value, and a length value.

22. The method of claim 21 wherein configuring further comprises:

asserting the execution mode word in a processor control register when the processor is configured in the isolated execution mode.

23. The method of claim 22 wherein asserting the isolated access signal comprises:

detecting if the physical address is within the isolated memory area defined by the isolated setting by an address detector.

24. The method of claim 23 wherein the isolated bus cycle is one of a data access cycle, a control access cycle, and a logical processor access cycle.

25. The method of claim 24 wherein the data access cycle is generated when the access type is a memory reference to the isolated memory area.

26. The method of claim 24 wherein the isolated register is in a chipset external to the processor.

27. The method of claim 26 wherein the control access cycle is generated when the access type is an input/output reference to the isolated register.

28. The method of claim 24 wherein the logical processor access cycle is generated when the access type is one of a logical processor entry to and a logical processor withdrawal from the isolated state.

29. The method of claim 28 wherein the logical processor entry to the isolated state updates a logical processor counter in the chipset in a first direction.

30. The method of claim 28 wherein the logical processor withdrawal from the isolated state updates a logical processor counter in the chipset in a second direction.

31. A system comprising:

a chipset;

a memory coupled to the chipset having an isolated memory area; and

a processor coupled to the chipset and the memory having an isolated bus cycle generator, the isolated bus cycle generator comprising:

a configuration storage containing configuration parameters to configure the processor in one of a normal execution mode and an isolated execution mode,

an access generator circuit coupled to the configuration storage to generate an isolated access signal using at least one of the isolated area parameters and access information in a transaction, the isolated access signal being asserted when the processor is configured in the isolated execution mode, and

a bus cycle decoder coupled to the access generator circuit to generate an isolated bus cycle corresponding to a destination in the transaction using the asserted isolated access signal and the access information.

32. The system of claim 31 wherein the configuration parameters include an isolated mode value and an execution mode word.

33. The system of claim 31 wherein the destination in the transaction is one of the isolated memory area, an isolated register, and an isolated state.

34. The system of claim 33 wherein the access information includes a physical address and an access type.

35. The system of claim 34 wherein the configuration storage comprises:

a register to contain the isolated setting for defining the isolated memory area.

36. The system of claim 35 wherein the isolated setting is one of a mask value, a base value, and a length value.

37. The system of claim 36 wherein the configuration storage further comprises:

a processor control register to contain the execution mode word, the execution mode word being asserted when the processor is configured in the isolated execution mode.

38. The system of claim 37 wherein the access generator circuit comprises:

an address detector to detect if the physical address is within the isolated memory area defined by the isolated setting.

39. The system of claim 38 wherein the isolated bus cycle is one of a data access cycle, a control access cycle, and a logical processor access cycle.

40. The system of claim 39 wherein the data access cycle is generated when the access type is a memory reference to the isolated memory area.

41. The system of claim 39 wherein the isolated register is in a chipset external to the processor.

42. The system of claim 41 wherein the control access cycle is generated when the access type is an input/output reference to the isolated register.

43. The system of claim 39 wherein the logical processor access cycle is generated when the access type is one of a logical processor entry to and a logical processor withdrawal from the isolated state.

44. The system of claim 43 wherein the logical processor entry to the isolated state updates a logical processor counter in the chipset in a first direction.

45. The system of claim 43 wherein the logical processor withdrawal from the isolated state updates a logical processor counter in the chipset in a second direction.

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